

Qualification Work

Bachelor | Research | Master Thesis

Development of a bevelled-edge semiconductor etching process for avalanche photodiodes

The Goal of this work

In this qualification work, a semiconductor etching process to produce bevelled-edge avalanche photodiodes has to be developed. For this, appropriate etching process parameters for Si, Ge and GeSn have to be found. Once the process parameters are calibrated some Si-based Avalanche Photodiodes are going to be fabricated and characterized to evaluate the influence of the bevel-edge angle to the dark current. During this work, you will gain a comprehensive insight into IHT's clean room technology as well as the electrical measurement technology.

Prior knowledge

Prior knowledge of semiconductor technology and/or measurement technology as well as experimental skills are an advantage.

Organizational

The topic of this qualification work can be developed into a bachelor, research or master thesis in terms of the scope and degree of the requirements.

Contact:

Maurice Wanitzek, M.Sc.

E-Mail: maurice.wanitzek@iht.uni-stuttgart.de

Tel.: +49 711 685-68023

Room: 1.412 im Pfaffenwaldring 47 (ETI II)

Dr. Michael Oehme

E-Mail: michael.oehme@iht.uni-stuttgart.de

Tel.: +49 711 685-68004

Room: 1.417 im Pfaffenwaldring 47 (ETI II)

Further tenders and information can be found at

www.iht.uni-stuttgart.de

IHT Competence field:
Photonics

Motivation

Avalanche Photodiodes are used in a broad spectrum of applications that need extremely high sensitivity e. g. telecommunication, lidar, or quantum photonics. To achieve this high sensitivity the devices must have good absorption while maintaining low noise. Due to the high electrical field at the semiconductor insulator interface, an avalanche multiplication of charge carriers can happen there. Since this interface typically has a lot of defects this mechanism is one main noise contributor of the devices.

To reduce this noise contributor, one has to decrease the electrical field on the interface while maintaining a sufficient electrical field in the bulk semiconductor. One possible way to do this is by etching the semiconductor mesa with a bevelled-edge. TCAD simulations which support this idea are shown in Figure 1.

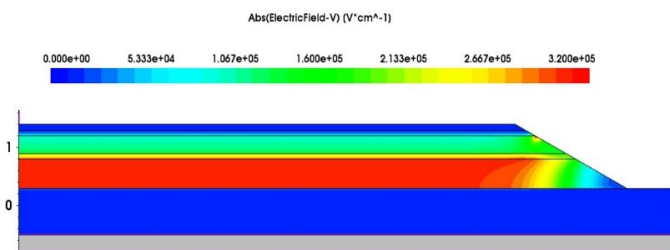


Figure: Electrical field simulations of a bevelled-edge avalanche photodiode structure show a field reduction at the semiconductor insulator interface

